PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)
Parruck et al.	) Docket No: COREP002D
Application No: Unknown	) Examiner: not assigned
Filed: February 9, 2001	) Group Art Unit: not assigned
For: SCHEDULING TECHNIQUES FOR DATA CELLS IN A DATA SWITCH	) Date: February 9, 2001

CERTIFICATE OF EXPRESS MAILING

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Diane Schwanbeck

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Before examination on the merits, please amend this divisional application as follows:

IN THE SPECIFICATION

Page 1, line 11-14: please delete "This application claims priority under 35 U.S.C. 119 (e) of a provisional application entitled "Asynchronous Switching Architectures Having Connection Buffers" filed October 28, 1996 by inventor Bidyut Parruck, et al. (U.S. Application No. 60/029,659)." and insert --This is a divisional

application of copending prior Application No. 08/872,530 filed on June 11, 1997, the disclosure of which is incorporated herein by reference.--

Page 10, line 18: after "ATM input port 309." please add --The ATM input ports 307 and 309 connect to the switch element 301 through a switch matrix input port 308 and a switch matrix input port 311 respectively.--

Page 22, line 25: before "In step 832" please add --The flowchart of Figure 8B starts with step 830 and continues to step 832.--

Page 23, line 5: after "the current iteration." please add --The flowchart of Figure 8C starts with step 860 and continues to step 862.--

Page 25, line 6: before "In step 932" please add --The flowchart of Figure 9A starts with step 930 and continues to step 932.--

Page 25, line 16: before "In step 962" please add --The flowchart of Figure 9B starts with step 960 and continues to step 962.--

Page 30, line 4: before "In step 1102" please add --The flowchart of Figure 11 starts with step 1100 and continues to step 1102.--

Page 34, line 12: before "In step 1402" please add --The flowchart of Figure 14 starts with step 1400 and continues to step 1402.--

Page 35, line 25: before "In step 1502" please add --The flowchart of Figure 15 starts with step 1500 and continues to step 1502.--

Page 36, line 7: before "In step 1602" please add --The flowchart of Figure 16 starts with step 1600 and continues to step 1602.--

IN THE CLAIMS

Please amend the claims as follows. All pending claims after this amendment are listed below for the convenience of the Examiner. Claims amended by the Amendment are indicated as such.

Please cancel claims 2-6.

1 (Amended) A [computer-implemented method for scheduling cells output on an output path of a] data switch [, said data switch being configured for switching said cells from a plurality of input paths to said output path, comprising] for communicating among a plurality of devices coupled to said data switch in a digital data network wherein a virtual connection is represented by a connection between a first device of said plurality of devices and a second device of said plurality of devices of said digital data network, said switch including:

[providing a plurality of queues, each queue of said plurality of queues having an assigned weight, respective ones of said plurality of input paths being coupled to respective ones of said plurality of queues;

providing a plurality of queues of queues, said plurality of queues being coupled to said plurality of queues of queues with queues of said plurality of queues having a similar weight being coupled a same queue of queues of said plurality of queues of queues; and

providing a scheduler, said plurality of queues of queues being input into said scheduler, said scheduler being coupled to said output path]

a switch element having a switch matrix;

at least one input switch access port structure coupled to said switch matrix containing a plurality of input back pressure buffer structures, wherein said plurality of input back pressure buffer structures is configured to allow input back pressuring to be accomplished on a per-virtual connection basis;

a plurality of input ports coupled to said at least one input switch access port structure, wherein said plurality of input ports are coupled to a plurality of traffic generators;

at least one output arbitration structure coupled to said switch matrix and coupled to said plurality of output ports, wherein said at least one output arbitration device represents the circuitry for arbitrating access to a single output port of said plurality of output ports; and

a plurality of output ports coupled to said output arbitration portion, wherein said plurality of output ports are coupled to a plurality of output destinations.

7. (New) The switch of claim 1 wherein a size of said plurality of input back pressure buffer structures are individually set.

8. (New) The switch of claim 1, wherein a size of a single input back pressure buffer structure of said plurality of input back pressure buffer structures is optimized by specifying a threshold window which includes a maximum and minimum size for said input back pressure buffer structure.

9. (New) The switch of claim 1, wherein a size of said plurality of input back pressure buffer structures is configured for a plurality of said virtual connections.

10. (New) The switch of claim 9, wherein said plurality of input back pressure buffer structures are configured for said plurality of virtual connections having a same priority.

11. (New) The switch of claim 1, wherein each output arbitration structure of said at least one output arbitration structure includes a plurality of schedulers and a plurality of selectors.

12. (New) The switch of claim 11, wherein each scheduler of said plurality of schedulers is configured to schedule ATM cells on one of a per-virtual connection basis, a per-port basis, a per traffic class, a per priority basis, a per group of virtual connections basis, and a cells similarly grouped basis.

13. (New) The switch of claim 11, wherein arbitration is performed on a per-virtual connection basis wherein said each scheduler of said plurality of schedulers are coupled to connections having a same priority for switching.

14. (New) The switch of claim 11, wherein each scheduler of said plurality of schedulers is coupled to at least two buffer structures having a same priority.

15. (New) The switch of claim 11 wherein each selector of said plurality of selectors is configured to select ATM cells using at least one of a round-robin selection technique and a weighted round-robin technique.

16. (New) The switch of 11, wherein said at least one output arbitration structure includes one of said plurality of selectors for every ATM output.

17. (New) A data switch for communicating among a plurality of devices coupled to said data switch in a digital data network wherein a virtual connection is represented by a connection between a first device of said plurality of devices and a second device of said plurality of devices of said digital data network, said switch including:

a switch element having a switch matrix;

at least one input switch access port structure coupled to said switch matrix containing a plurality of input back pressure buffer structures, wherein said plurality of input back pressure buffer structures is configured to allow input back pressuring to be accomplished on a per-virtual connection basis;

a plurality of input ports coupled to said at least one input switch access port structure, wherein said plurality of input ports are coupled to a plurality of traffic generators; and

at least one output switch access structure coupled to said switch matrix, said at least one output switch access structure including,

a plurality of schedulers,

a at least one selector,

an at least one switch matrix output port; and

at least one output port coupled to said at least one output switch access structure, wherein said at least one output port is coupled to a plurality of output destinations;

wherein said at least one output switch access structure arbitrates access to a respective said at least one output port.

18. (New) The switch of claim 17 wherein a size of said plurality of input back pressure buffer structures are individually set.

19. (New) The switch of claim 18 wherein a size of a single input back pressure buffer structure of said plurality of input back pressure buffer structures is optimized by specifying a threshold window which includes a maximum and minimum size for said input back pressure buffer structure.

20. (New) A data switch for communicating among a plurality of devices coupled to said data switch in a digital data network wherein a virtual connection is represented by a connection between a first device of said plurality of devices and a second device of said plurality of devices of said digital data network, said switch including:

a switch element having a switch matrix;

at least one input switch access port structure coupled to said switch matrix containing a plurality of input back pressure buffer structures, wherein said plurality of input back pressure buffer structures is configured to allow input back pressuring to be

accomplished on a per-virtual connection basis, and a size of a single input back pressure buffer structure of said plurality of input back pressure buffer structures is optimized by specifying a threshold window which includes a maximum and minimum size for said input back pressure buffer structure, and a size of said plurality of input back pressure buffer structures are individually set;

a plurality of output switch access port structures coupled to said switch matrix;

a plurality of input ports coupled to said plurality of switch access port structures, wherein said plurality of input ports are coupled to a plurality of traffic generators;

a plurality of output ports coupled to said switch matrix, wherein said plurality of output ports are coupled to a plurality of output destinations; and

at least one output arbitration device coupled to said switch matrix and coupled to said plurality of output ports, wherein said at least one output arbitration device represents the circuitry for arbitrating access to a single output port of said plurality of output ports.

21. (New) The switch of claim 20, wherein said at least one output arbitration device schedules cells inputted into said input ports in accordance to a weight accorded to each cell of said plurality of cells.

22. (New) A switch element, comprising:

an input routing portion including a switch matrix input port for receiving data;

a buffer portion including a plurality of buffers;

a switch matrix portion for routing data out from the plurality of buffers;

an output arbitrating portion, including,

a plurality of schedulers for receiving the data from the plurality of buffers through the switch matrix,

a selector for receiving data from the plurality of schedulers, the selector enabling output from the switch element through a switch matrix output port.

23. (New) A switch element as recited in claim 22, further comprising:

an additional input routing portion including an additional switch matrix input port for receiving data;

an additional buffer portion including an additional plurality of buffers, the switch matrix portion routing data out from the additional plurality of buffers;

an additional output arbitrating portion, including an additional plurality of schedulers for receiving the data from the additional plurality of buffers through the additional switch matrix, and

an additional selector for receiving data from the additional plurality of schedulers, the additional selector enabling output from the switch element through an additional switch matrix output port.

24. (New) A switch element as recited in claim 23, wherein the output arbitrating portion receives data from the buffer portion and the additional buffer portion through the switch matrix portion and the additional switch matrix portion.

25. (New) A switch element as recited in claim 24, wherein the additional output arbitrating portion receives data from the buffer portion and the additional buffer portion through the switch matrix portion and the additional switch matrix portion.

26. (New) A switch element as recited in claim 22, wherein the input routing portion receives data from a plurality of traffic generators.

27. (New) A switch element as recited in claim 23, wherein a plurality of traffic acceptors receive data from the output arbitrating structure.

28. (New) A switch element, comprising:

a first input routing portion including a first switch matrix input port for receiving data;

a first buffer portion including a first plurality of buffers;

a switch matrix portion for routing data out from the first plurality of buffers and a second plurality of buffers;

a first output arbitrating portion, including,

a first plurality of schedulers for receiving the data from the first plurality of buffers and the second plurality of buffers through the switch matrix,

a first selector for receiving data from the first plurality of schedulers, the first selector enabling output from the switch element through a first switch matrix output port;

a second input routing portion including a second switch matrix input port for receiving data;

a second buffer portion including the second plurality of buffers;

a second output arbitrating portion, including,

a second plurality of schedulers for receiving the data from the first plurality of buffers and the second plurality of buffers through the switch matrix,

a second selector for receiving data from the second plurality of schedulers, the second selector enabling output from the switch element through a second switch matrix output port;

a plurality of traffic generators for inputting data into the first input routing portion and the second input routing portion; and

a plurality of traffic acceptors to receive data from the first output arbitrating portion and the second output arbitrating portion.

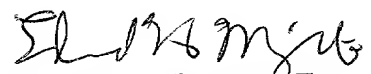
REMARKS

Claims 2-6 have been canceled. New claims 7-28 have been added. Claims 1 and 7-28 are pending after entry of the present Preliminary Amendment. The claims containing the subject matter of this Divisional Application was canceled in the parent case, United States Patent Application Serial No. 08/872,530, due to a restriction requirement imposed by the Examiner. Amendments were made to the claim 1 to better define that which the Applicants consider to be the invention and to incorporate the subject matter the parent application that was subject to the restriction requirement by the Examiner. New claims 7-28 that incorporate the subject matter of the parent application that was subject to the restriction requirement by the Examiner have been added. The Applicants submit that no new matter has been added by the amendment of claim 1 and the addition of claims 7-28, and further submit that all of the pending claims are supported by the specification.

The Applicants respectfully request examination on the merits of the subject application, and respectfully submit that all of the pending claims are in condition for allowance. Accordingly, a notice of allowance is respectfully requested. If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to

contact the undersigned at (408) 749-6900. If any additional fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. COREP002D).

Respectfully submitted,
MARTINE PENILLA & KIM, L.L.P.



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